LISTING OF THE CLAIMS

The following Listing of the Claims replaces all prior listings of the claims within this application.

1. (canceled)

2. (previously amended) The method of claim 16 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. (previously amended) The method of claim 16 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. (previously amended) The method of claim 16 wherein the second substrate is a second semiconductor substrate.

5. (previously amended) The method of claim 16 wherein the first semiconductor substrate is thicker than the second substrate.

6. (previously amended) The method of claim 16 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

7. (original) The method of claim 6 wherein each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3000 to about 6000 angstroms.

8. (previously amended) The method of claim 16 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

9. - 11. (canceled)

12. (previously amended) The method of claim 16 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. (previously amended) The method of claim 16 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

14. - 15. (canceled)

16. (previously added) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, where the removal method employs the dielectric isolated metallization pattern as a stop layer.